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Complete if Known

Application Number	09/931,131
Filing Date	August 16, 2001
First Named Inventor	Hyungwon Kim, et al.
Group Art Unit	2812
Examiner Name	

Attorney Docket Number UOM 0209 PUSP

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>HW</i>		DAMIANI, MAURIZIO, ET AL, Optimization of Combinational Logic Circuits Based on Compatible Gates, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 14, No. 11, November 1995.	
<i>HW</i>		STANION, TED, ET AL, Boolean Division and Factorization Using Binary Decision Diagrams, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 13, No. 9, September 1994, pgs. 1179-1184.	
<i>SH</i>		MINATO, SHIN-ICHI, Fast Factorization Method For Implicit Cube Set Representation, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 15, No. 4, April 1996, pgs. 377-384.	
<i>SH</i>		PAL, AJIT, ET AL, Synthesis of Two-Level Dynamic CMOS Circuits, IEEE, 1999, pgs. 82-92.	
<i>SH</i>		BEAYTON, ROBERT K., ET AL., MIS: A Multiple-Level Logic Optimization System, IEEE Transactions on Computer-Aided Design, Vol. CAD-6, No. 6, November 1987, pgs. 1062-1081.	

Examiner Signature

Jay Lee

Date Considered

4/23/03

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